TO: John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)

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IEEE P1285 Liaison to X3T9.2/DADI
Apple Computer

Date: February 15, 1993

Subject: P1285 Liaison Report for February 1993

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- Control and data space is memory mapped using P1212
- One controller, multiple slaves model
- Byte addressable, true memory mapped disk architecture
- Inherent spindle synchronization support
- Isochronous support
- Live insertion/removal
- Motherboard direct attach
- Scalability in performance and cost

IEEE P1285 Project Status

In order to reduce the number of packets on the RAMLink bus, Martin proposed a "super packet" concept. It simply increases the maximum data size in a packet from 64 bytes to 512 bytes. The final decision on this issue was not made for that it requires a change to the RAMLink document. The group agreed that further investigation would be required before accepting the proposal.

The discussion of where the functional boundary lies between the alpha and beta levels continues. Conceptually, the beta level can be viewed as the HBA interface;

and the alpha level, as the disk interface. The functional division between the two levels is currently defined as follows:

alpha	beta
• low overhead	• memory mapped
• minimal buffer	• caching
• ECC-on-the-fly	• DMA
• synchronous command processing	• Command queuing
• spindle synchronization	• I/O scheduling

The goal of the alpha level is to create a low-overhead, efficient read/write engine with most of the intelligence/features pushed up to another level. The goal of the beta level is to provided added features (memory mapped, read-ahead, etc.).

The physical layer and the interface definition for the alpha level are being discussed with no concensus yet.

The P1285 reflector is up and running. The monthly meeting minutes and announcements are posted on the reflector. People who want to receive information from the reflector should contact Dennis Pak at 'dennis.pak @applelink.apple.com'.

Third Grass Roots Meeting

The third grass roots meeting was held on January 14, 1993, at the Santa Clara University, Santa Clara, CA. The following statements summarize the outcomes of the meeting:

• Better coordination by scheduling co-located meetings with X3T9 to encourage participation from the X3T9 members.
• No consensus on the development ownership of "alpha" and "beta".

Both IEEE and ANSI officials were invited to the meeting. However, none showed up.

Upcoming Events

• P1285 tentative meeting dates and locations (First Thursday of every month):

March	3/4/93	@Apple Computer, 1 Infinite Loop, Cupertino
April	4/1/93	@Santa Clara University, Bannon Engineering Bld.
*May	5/20/93	*@Co-located meeting with X3T9 in Santa Fe, NM.*
June	6/3/93	@Santa Clara University, Bannon Engineering Bld.

* Note: This is tentative. Please contact Martin Freeman at a later time.

These meetings are scheduled from 2:00-5:00 PM. Please contact Martin Freeman at (415)354-0329 for exact date and location, or for additional information.